Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–I(New course)• EXAMINATION – WINTER- 2015

Subject Code: 2715401 **Date: 01/01/2016**

Subject Name: ARM Processor Architecture and System Design

Time:2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions. **07**

1) What is the content of CPSR register just after reset?
2) What kind of instruction is expected at 0x00000000 memory location in ARM processors?
3) Write down two pseudo instructions in ARM processor.
4) What will happen if a 32 bit machine code fetched from memory is not in the list of available machine codes?
5) In which mode ARM cpu will be working just after the reset?
6) What is the role of 'Incrementer' block in ARM CPU architecture?
7) Write down an instruction to return from a subroutine.

(b) Answer the following questions. **07**

1) Explain fully ascending stack operation in ARM CPU.
2) What is CPI in ARM processor terminology? Describe the approaches on architecture level to improve CPI.

Q.2 **(a)** Let there be a 16 bit array with 10 elements. It is required to identify the index associated with 16 bit specific value present in the array. Write an ARM assembly language program to identify the index of an element defined in register R0. **07**

(b) What is the difference between a subroutine and a SWI call? Explain how SWI instruction will be executed to serve several service calls with an example. **07**

OR

(b) Explain all the types of Branch and Link instructions in THUMB mode. **07**

Q.3 **(a)** Answer the following questions related to the Phase Locked Loop in LPC2148. **07**

(1) How can you bypass the PLL and drive CPU core with Crystal Frequency?
(2) If Crystal Frequency is of 10 MHz, what should be the setting of registers associated with PLL for CCLK as 60 MHz?
(3) What is the significance of PLL feed sequence?

(b) Explain the ARM Bus Structure with types of Buses and their requirements. **07**

OR

Q.3 **(a)** Describe the use of Match Registers in association with Match Pinouts for **07**

toggling the Match Pin in LPC2148?

	(b)	Explain the use of Vector Interrupt Controller for configuring the External Interrupt pin as vectored interrupt request in LPC2148?	**07**
Q.4	**(a)**	Describe the use of Timer Registers and Match Register for providing digital data to Digital to Analog Convertor at the rate of 1 KHz.	**07**
	(b)	Describe the use of ADC registers for scanning six analog channels in ECG signal acquisition.	**07**

OR

Q.4	**(a)**	Explain the use of ADC Control Register in detailed manner for configuring ADC for analog signal acquisition.	**07**
Q.4	**(b)**	Describe the use of Alarm Registers in association with Time Counter Registers in the Real Time Clock module.	**07**
Q.5	**(a)**	What are the requirements of Watch dog timer in Embedded Systems? Describe all the possible modes of operation in association with Watch dog timer in LPC2148.	**07**
	(b)	Explain Single Edge PWM operation with the help of PWM modulator along with the use of Timer registers.	**07**

OR

Q.5	**(a)**	Describe the use of Data and Remote frames in CAN bus protocol.	**07**
	(b)	Explain the I^2C bus protocol implemented in LPC 2148 describing the use of I^2C Control Register.	**07**

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