Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–I(New course)• EXAMINATION – WINTER- 2015

Subject Code: 2715410 **Date: 04/01/2016**

Subject Name: Advanced Digital Circuit Design

Time:2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	List the different level of abstraction in digital design also discuss various digital circuit design implementation approaches.	**07**
	(b)	Defined module instance? Draw the block-diagram and write Verilog code for 4 bit ripple carry full adder Using one bit full adders.	**07**
Q.2	**(a)**	Discuss Synthesis and Technology mapping for FPGA in detail	**07**
	(b)	Briefly discuss delay based and event based timing control in Verilog.	**07**
		OR	
	(b)	What do you understand by Gate Delays? Compare Rise Delay and Fall Delay with suitable examples and waveforms**.**	**07**
Q.3	**(a)**	Explain Blocking and Non-Blocking statements with suitable examples	**07**
	(b)	List various Operator types. Discuss any two in detail.	**07**
		OR	
Q.3	**(a)**	Discuss data types used in Verilog in brief.	**07**
	(b)	Defined component of simulation. Write Verilog code to design Edge triggered D flip flop	**07**
Q.4	**(a)**	Write short note on hardware-software co-design	**07**
	(b)	Discuss brief about sequential circuit design also write the Verilog code for Ring counter	**07**
		OR	
Q.4	**(a)**	Write a Verilog code for BCD to Seven segment convertor	**07**
	(b)	Discuss concept of Floor Planning in detail.	**07**
Q.5	**(a)**	Briefly Discuss the two level optimization of combinational circuits	**07**
	(b)	Briefly Discuss Placement and Routing.	**07**
		OR	
Q.5	**(a)**	Briefly discuss techniques for Partitioning.	**07**
	(b)	What is the difference between Moore and Mealy finite state machines? Write Verilog code for Traffic light controller.	**07**

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