Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–II(New course)• EXAMINATION (Remedial) – WINTER- 2015

Subject Code: 2720314 **Date: 10/12/2015**

Subject Name: ADVANCE VLSI DESIGN

Time: 2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the timing diagram observed while simulating the design of x^4 implementation of Iterative architecture in Xilinx ISE that shows all signals observed in simulation window and justifies functionality of the design. State throughput, latency and timing of your design with proper justification.	**10**
	(b)	Write the Verilog program using Data flow modeling for 2 to 4 Decoder	**04**
Q.2	**(a)**	Explain Register Balancing for timing in Architecting Speed.	**07**
	(b)	Write verilog code to design a 4-bit adder using full adder and half adder. Use gate level modeling for half and full adders.	**07**
		OR	
	(b)	Write a Verilog program for UDP of 2 to 1 MUX	**07**
Q.3	**(a)**	Implement the function $Y = AX^4 + BX^3 + CX^2 + DX + E$ in verilog considering maximum time delay in the critical path of one 8 bit x 8 bit multiplier delay only. Assume A, B, C, D,E, X, and Y of 8-bit. Draw implementation diagram of the same. What is the throughput and latency of your design?	**14**
		OR	
Q.3	**(a)**	Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "101 0" input bit sequence. Implement the state diagram for above and write verilog code for it.	**14**
Q.4	**(a)**	Write the Verilog program for find Factorial using Behavior Modelling.	**07**
	(b)	Write the Verilog program for 8-bit ALU using Behavior Modelling.	**07**
		OR	
Q.4	**(a)**	Write verilog program and test bench for full subtractor.	**07**
	(b)	Write the Verilog program for data fatch from ROM using Behavior Modelling.	**07**
Q.5	**(a)**	Write verilog code to implement following arithmetic (addition) operation. Y <= A + B if S1=0 and S0=0 Y <= B + C if S1=0 and S0=1 Y <= A + C if S1=1 and S0=0 Draw implementation diagram of the above with and without resource sharing option in synthesis tool. What is the advantage and limitation of using resource sharing in this implementation?	**14**
		OR	
Q.5	**(a)**	Design a counter with a binary sequence 0, 3, 2, 5, 7, 6, 0, 3, 2, … using T flipflop. Asynchronous reset when activated, resumes counter with 0. Show all design steps. Write verilog program of the same using structural modeling style. Write verilog programs of all components used in the design. Using a test bench verify the counter design	**14**