Seat No.: _____ Enrollment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER– II • EXAMINATION – WINTER 2015

Subject Code: 2724202 **Date: 09/12/2015**

Subject Name: Testing & Verification of VLSI Design

Time: 02:30 PM – 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all the questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Notations and symbols used have usual technical meaning.**

Q.1	**(a)**	List down the various type of cost for Testing and explain each in brief.	**07**
	(b)	What is Defect in Testing? List down and explain the different types of Defect? Prepare the table for Printed Circuit Board (PCB) Defect.	**07**
Q.2	**(a)**	Prepare and explain the table which gives summary of Modeling Levels and Simulator.	**07**
	(b)	What do you mean by ATPG? Explain the Path Sensitization Method.	**07**
		OR	
	(b)	Explain in Brief (a) Controllability (b) Design for Verification (c) Fault Modeling.	**07**
Q.3	**(a)**	What do you mean by Testing Philosophy? Explain it with example of Testing the Students.	**07**
	(b)	Discuss the Test Program with suitable diagram.	**07**
		OR	
Q.3	**(a)**	What are the advantages of Third Party Model? Discus in detail.	**07**
	(b)	Which are the various levels of verification? Explain each in Brief.	**07**
Q.4	**(a)**	What is the difference between Functional and Structural Testing?	**07**
	(b)	What is Linting Tools? Discuss the limitations of Linting Tools.	**07**
		OR	
Q.4	**(a)**	Explain Scan Design with Example of D Flip Flop.	**07**
	(b)	What is BITS? Explain BITS Pattern Generation.	**07**
Q.5	**(a)**	How can you differentiate the Verification form Testing?	**07**
	(b)	With Suitable Diagram explain the Basic Principal of IDDQ testing.	**07**
		OR	
Q.5	**(a)**	Discuss the Test Time Complexity for Memory Testing.	**07**
	(b)	List down the various types of Delay Test Methodologies? Discuss each in Brief.	**07**

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