Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II(New course) • EXAMINATION (Remedial) – WINTER- 2015

Subject Code: 2724204 Date: 11/12/2015

Subject Name: HDL Based Design with Programmable Logic

Time:2:30 pm to 5:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks**

Q.1 **(a)** Do as directed. (Each carry 1 Mark) **07**

1. Declare an enumerated data type called WEEKDAYS containing all week days.
2. What are the logic levels supported by STD_LOGIC data type?
3. Declare an entity for 4 bit adder circuit.
4. The syntax and semantics of Verilog are similar to which sequential programming language?
5. What is the difference between a Transaction and an Event?
6. Write a declaration statement to define an 8bit data bus.
7. What is the priority level of different branches in the CASE statement?

(b) State True/False. (Each carry 1 Mark) **07**

1. The order of execution of sequential VHDL statements can be predicted.
2. Conditional assignment statements can be used outside process statement.
3. Process statement itself is concurrent.
4. BIT data type is similar to STD_LOGIC.
5. The assignment to Variable in VHDL is updated immediately.
6. The element of an Array in VHDL can be another Array.
7. An object of type Record may contain elements of different types.

Q.2 **(a)** What are the different levels of abstraction in VLSI design? **07**

(b) Explain various types of delays in VHDL. **07**

OR

(b) Write a short note on CASE statement. **07**

Q.3 **(a)** Realize following functions using PLA. What is the minimum size of PLA required to implement? **07**

$F_1 = \sum(0,1,4,6)$

$F_2 = \Sigma(2,3,4,6,7)$

$F_3 = \sum(0,1,2,6)$

$F_4 = \sum(2,3,5,6,7)$

(b) Name different FPGA device families manufactured by Xilinx. What are the architectural features available in latest FPGA devices? **07**

OR

Q.3 **(a)** Compare following ï **07**

1. PLA vs. ROM 2. FPGA vs. CPLD

(b) Compare merits and demerits of full custom versus semicustom design style. **07**

Q.4 **(a)** Write a VHDL description for the state machine to count from 0 to 9 using FSM design style. **07**

(b) 1. Explain the need of resolution function in VHDL. (3 Marks) **07**
2. What is VHDL? What are its capabilities and usage? (4 Marks)

OR

Q.4 **(a)** Define Event-Driven Simulator and Cycle-Based Simulators. Discuss the operation of Cycle Based Simulator with suitable example. **07**

(b) Write a complete test bench using VHDL to test 3x8 decoder with active high enable i/p EN. **07**

Q.5 **(a)** Do as directed - **07**
1. What are the pros & cons of HDL over Schematic based design entry? (3 Marks)
2. What the role is of TRANSLATE, MAP and PLACE & ROUTE tools in FPGA based design flow? (4 Marks)

(b) Write the VHDL code to describe the digital circuit given in Figure 1. **07**

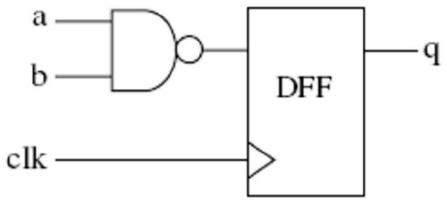

Figure 1

OR

Q.5 **(a)** Explain the use of following VHDL constructs ï **07**
a. GENERIC
b. GENERATE

(b) Discuss with example - various types of modeling styles supported in VHDL. **07**

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