Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. SEMESTER III–EXAMINATION – WINTER 2015

Subject code: 2732605 **Date: 04/12/2015**

Subject Name: VLSI Test principles and Architectures

Time: 2:30 PM to 5:00 PM **Total Marks: 70**

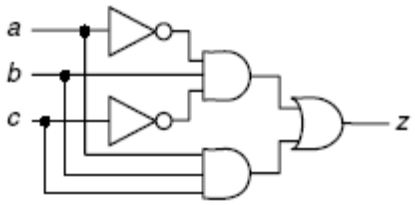
Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 (a) Do as Directed: **07**

1. Compare Yield and Reject Rate.
2. Explain Scan Stitching in brief in design and testability.
3. Briefly explain event-driven simulation.
4. Define Golden Signature.
5. Define robustly testable path.
6. Briefly explain IDDQ Testing.
7. Define One-Hot Skewed-Load.

(b) Consider the combinational logic circuit in following figure. How many possible single stuck-at faults does this circuit have? How many possible multiple stuck-at faults does this circuit have? How many collapsed single stuck-at faults does this circuit have? **07**



Q.2 (a) Discuss test point insertion in DFT. **07**

(b) Explain logic simulation for design verification. **07**

OR

(b) List out commonly used gate and wire delay models and describe any two of these. **07**

Q.3 (a) Draw and explain typical scan design flow. **07**

(b) Explain Random Test generation. **07**

OR

Q.3 (a) Briefly explain event driven simulation. **07**

(b) Explain PODEM algorithm (No need to separately write Pseudo codes). **07**

Q.4 (a) Draw structure of Standard and Modular LFSR and compare both with example. **07**

(b) What is Output Response Analysis? Explain different output response compaction techniques. **07**

OR

Q.4 (a) Briefly explain Untestable Fault Identification. **07**

(b) Draw and explain snap-shot scan design architecture. **07**

Q.5 (a) Classify the BIST techniques and draw block diagram of logic BIST system and explain it. **07**

(b) Define Hazard and explain static Hazard detection. **07**

OR

Q.5 (a) List out BIST design rules and explain any three in detail. **07**

(b) Discuss Spectrum-Based ATPG. **07**