Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. SEMESTER III–EXAMINATION – WINTER 2015

Subject code: 2734203 Date: 04/12/2015

Subject Name: High Speed CMOS VLSI Circuit

Time: 2:30 PM to 5:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain inter-Die variation in detail.	**07**
	(b)	List out Fail causes and explain it.	**07**
Q.2	**(a)**	Find the Elmore delay the nodes Vout3 and Vout4 in the RC tree shown in Fig. 1.	**07**
	(b)	Calculate the Elmore delay from In to Out1 and from In to Out2 from fig.2. Which one is critical path? Assume R = 100Ω and C = 10fF. Calculate the Elmore delay of the critical path that you found.	**07**
		OR	
	(b)	Explain power optimization for high speed VLSI circuit.	**07**
Q.3	**(a)**	Explain Static CMOS Structure in detail with diagram and its type.	**07**
	(b)	Explain Domino CMOS in detail with diagram.	**07**
		OR	
Q.3	**(a)**	Explain Self-Resetting Domino Structure (SRCMOS) on detail.	**07**
	(b)	Explain differential Domino Structure with diagram.	**07**
Q.4	**(a)**	Explain Clocked Pass –Gate Logic in detail with diagram and its type.	**07**
	(b)	List out Latched Domino structure and explain Simple set Differential logic (SSDL).	**07**
		OR	
Q.4	**(a)**	List out latching single-ended logic types and explain double edge triggered flip-flops (DETFF) with necessary diagrams.	**07**
	(b)	Write a short note on latch clocking.	**07**
Q.5	**(a)**	List out latching single-ended logic types and explain Differential cascode voltage switch(DCVS) latch with necessary diagrams	**07**
	(b)	Write a short note on race free latches for Pre charged logic.	**07**
		OR	
Q.5	**(a)**	Explain Circuit optimization techniques for high speed VLSI circuit.	**07**
	(b)	Explain any one mathematical optimization techniques.	**07**

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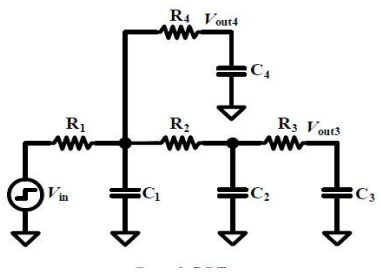

Fig.1

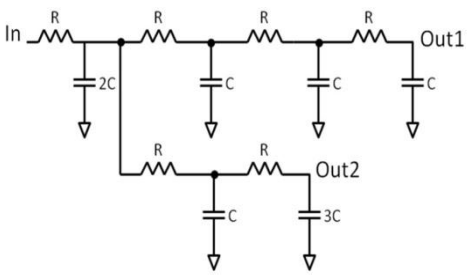

Fig.2