Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–I(New course)• EXAMINATION – WINTER- 2015

Subject Code: 3715204 **Date: 05/01/2016**

Subject Name: Digital VLSI Design & Verification-I

Time:2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Design FSM for level to pulse converter. Level to pulse converter has to produce a single-cycle pulse each time when its input goes high.	**07**
	(b)	Explain glitches in digital design? How to avoid it.	**07**
Q.2	**(a)**	What is metastability? What are different cases metastability occurs? How to avoid metastability for high-speed systems and also write the equation for MTBF.	**07**
	(b)	Explain the different between blocking and non-blocking assignment in Verilog, variable and signal in VHDL with examples.	**07**
		OR	
	(b)	Explain tasks and functions in Verilog with one example for each. What do you mean by re-entrant tasks?	**07**
Q.3	**(a)**	Explain ASIC design flow in detail.	**07**
	(b)	Explain transport delay, inertial delay and delta delay in VHDL with example.	**07**
		OR	
Q.3	**(a)**	Explain different design challenges in VLSI.	**07**
	(b)	Write a note on design economics related to IC.	**07**
Q.4	**(a)**	Draw the layout for 2-input XOR gate and 4-input NOR gate.	**07**
	(b)	Write the Verilog code for universal shift register.	**07**
		OR	
Q.4	**(a)**	What is FPGA? Mention the different software used in XILINK ISE. Compare the ASIC, FPGA and micro controller in terms of performance, NRE cost, unit cost and time to market.	**07**
	(b)	Write the Verilog code and System Verilog assertions for the asynchronous FIFO.	**07**
Q.5	**(a)**	What is interfaces in system Verilog? Explain the advantage of interface with one example.	**07**
	(b)	Explain inheritance, encapsulation and polymorphism in System Verilog with example.	**07**
		OR	
Q.5	**(a)**	Explain different types of ASIC in detail.	**07**
	(b)	What is assertions? Explain different concurrent assertion layers with example.	**07**

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