Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME - SEMESTER– II(New course) • EXAMINATION (Remedial) – WINTER- 2015**

**Subject Code: 3725203** **Date: 10/12/2015**

**Subject Name: Digital VLSI Design-II**

**Time:2:30 pm to 5:00 pm** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | Explain ASIC physical design flow in detail. | **07** |
| | **(b)** | What are constraints? Explain optimization constraints and design rule constraints. | **07** |
| **Q.2** | **(a)** | Explain various kinds of libraries that will be used during Physical design flow? | **07** |
| | **(b)** | What do you understand by Retention Register? When you will use these retention register? | **07** |
| | | **OR** | |
| | **(b)** | Explain routing operation with flow graph and briefly explain each step. | **07** |
| **Q.3** | **(a)** | What are different clock distribution styles? Explain any one of them in detail. | **07** |
| | **(b)** | What is crosstalk? Why we have crosstalk issue? What kind of problems are induced due to crosstalk. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | List Different types of Wire Load Modes? Explain any one of them. | **07** |
| | **(b)** | What is congestion? Explain how to analyses and fix congestion. | **07** |
| **Q.4** | **(a)** | What are the steps involved while designing Hierarchical floor-plan? | **07** |
| | **(b)** | Draw block diagram of output buffer. Explain each block in brief. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | What is critical path? At what point in the design flow can one first find out about critical paths? Explain the role of clock skew, setup and hold times in sequential circuits. | **07** |
| | **(b)** | Explain different paths you analyze while performing static timing analysis. | **07** |
| **Q.5** | **(a)** | Explain with two examples how there is a possibility to get synthesis simulation mismatch. | **07** |
| | **(b)** | Explain signal integrity issues in VLSI design. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | What are the two methodologies to achieve power planning? List steps to obtain good power planning. | **07** |
| | **(b)** | Draw Y-chart and explain it. | **07** |

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