Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– III • EXAMINATION – WINTER 2015

Subject Code: 3735203 **Date: 07/12/2015**

Subject Name: Verification Methodology

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare system Verilog with other HDL. Why use system Verilog for verification.	**07**
	(b)	Explain universal verification components in details.	**07**
Q.2	**(a)**	List of developing reusable components and explain any three in details	**07**
	(b)	Importance of Make file, Perl scripting, TCL scripting in verification.	**07**
		OR	
	(b)	What exactly is the difference between OVM, UVM, and VMM verification methodologies, and what do they signify?	**07**
Q.3	**(a)**	What is UPF? What does it Do? How is it put in to action? What support it?	**07**
	(b)	Write a program and possible test case for AND gate use system Verilog language	**07**
		OR	
Q.3	**(a)**	What is the regression and importance of regression in verification methodology	**07**
	(b)	What is Universal Verification Methodology (UVM) in layman's terms?	**07**
Q.4	**(a)**	Explain Register model used in verification environment.	**07**
	(b)	Explain block level testing and chip level testing in details.	**07**
		OR	
Q.4	**(a)**	Explain development of ARM/MIPS BFM.	**07**
	(b)	Explain concurrent and immediate assertion in details.	**07**
Q.5	**(a)**	What is the difference between functional verification and RTL verification?	**07**
	(b)	Explain blocking and non-blocking assignment in system Verilog with suitable programs.	**07**
		OR	
Q.5	**(a)**	Write a short not on functional coverage.	**07**
	(b)	Write a short note on TLM.	**07**

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