Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– III• EXAMINATION – WINTER 2015

Subject Code:3735206 **Date: 07/12/2015**

Subject Name: Embedded Computing

Time: 02:30 PM to 05:00 **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain how different types of compatibilities decide the distinction between embedded systems and non-embedded systems.	**07**
	(b)	Explain how the technology trend has changed the SoC design over the years in terms of process technology, cost, complexity and applications.	**07**
Q.2	**(a)**	Explain in detail the design philosophy of VLIW in comparison to Superscalar and DSP architecture.	**07**
	(b)	Explain how by passing logic works in VLIW architecture with the help of suitable diagram	**07**
		OR	
	(b)	Explain key aspects of a processor's hardware that enable ILP	**07**
Q.3	**(a)**	How pipeline is balanced while designing a pipeline architecture	**07**
	(b)	Explain how forwarding logic works in VLIW architecture with the help of suitable diagram.	**07**
		OR	
Q.3	**(a)**	Explain some features of individual caches in the cache hierarchy which are implemented in today's cache controller.	**07**
	(b)	What are the factors that complicate real world implementation of cache design in parallel processor architecture?	**07**
Q.4	**(a)**	Compare interpreted simulators and compiled simulators. What are the advantages and disadvantages of both.	**07**
	(b)	Explain the process of Dynamic Binary Translation System with the help of suitable diagram.	**07**
		OR	
Q.4	**(a)**	Explain advantages and disadvantages of Trace-driven simulators.	**07**
	(b)	Explain how Discrete Event Simulation works when Hardware Simulation is being employed.	**07**
Q.5	**(a)**	List down and explain the compiler-visible features of DSP.	**07**
	(b)	What are acyclic region types and how they are used in deciding Instruction scheduling in ILP. Explain the difference between Treegion and Trace2 regions with a diagram	**07**
		OR	
Q.5	**(a)**	Describe a typical code compression system with suitable diagram.	**07**
	(b)	Describe how Firmware upgrades are downloaded on Embedded devices	**07**

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