Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. SEMESTER I (old course)–EXAMINATION (Remedial) – WINTER 2015

Subject code: 710403N **Date: 10/12/2015**

Subject Name: SIC Design

Time: 10:30 AM to 1:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Do as Directed **1)** Give difference between signal and variable **2)** What is an OTP FPGAs? **3)** What is signal driver? **4)** Discuss Test Bench. **5)** Difference between Concurrent & Sequential Statement **6)** Explain óWait statementô **7)** Define the terms :Regularity & Modularity	**14**
Q.2	**(a)**	Explain the ASIC Design Flow.	**07**
	(b)	Describe Delay in VHDL.	
		OR	
	(b)	What are the eight types of ASICs? List them and Describe any two in detail.	**07**
Q.3	**(a)**	Discuss fuse, antifuse and SRAM programming methods of FPGA.	**07**
	(b)	Explain transport delay model and inertial delay model. Also give comparison between them.	**07**
		OR	
Q.3	**(a)**	Implement the following Equation using Structural & Data Flow modelling Y=ABC+ADE+DEC	**07**
	(b)	Write VHDL Code for 1) 4 X 1 DMUX using WITH/SELECTstatement 2) 1X 8 MUX using Case statement	**07**
Q.4	**(a)**	What is the need of Floor Planning?List the major Objective of Floor Planning	**07**
	(b)	Write VHDL code for a Sequence detector of Sequence ñ1010ò.Also Draw State Diagram	**07**
		OR	
Q.4	**(a)**	Explain XC5200 Xillinx logic block.How many input can be handled by it?	**07**
	(b)	Discuss types of Finite State Machine with appropriate Example	**07**
Q.5	**(a)**	Write a short note on Operators used in VHDL	**07**
	(b)	Write a VHDL code for 4 Bit Parallel ï In-Serial-out Shift Register	**07**
		OR	
Q.5	**(a)**	Discuss various Loops in VHDL and Explain óGenerateô Statement.	**07**
	(b)	Explain Programmable Logic devices. Also Give Comparison between PAL,PLA, CPLD and FPGA	**07**

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