Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. SEMESTER III–EXAMINATION (Remedial)– WINTER 2015

Subject code: 730303 **Date: 07/12/2015**

Subject Name: VLSI Design

Time: 2:30 PM to 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "11001" input bit sequence. Implement the state diagram for above and write verilog code for it.	**14**
Q.2	**(a)**	Define a negative-edge triggered T flipflop with clear as a UDP. Signal clear is active low.	**07**
	(b)	How begin-end and fork-join block differs in execution? Explain with example along with waveforms.	**07**
		OR	
	(b)	Explain gate delays in detail.	**07**
Q.3	**(a)**	How do sequential and parallel blocks vary in processing? Explain with the help of example.	**07**
	(b)	Write verilog program for 4-bit up-down counter with load facility. Draw the circuit diagram for the same.	**07**
		OR	
Q.3	**(a)**	Explain mux- versus LUT-based logic blocks.	**07**
	(b)	Write a verilog program of 16-to-1 multiplexer using conditional operator.	**07**
Q.4		Explain in detail configuration modes of FPGA.	**14**
		OR	
Q.4		Explain in detail the architecture of XC9500 Complex Programmable Logic Devices.	**14**
Q.5		With the help of T flipflop, design modulo-13 counter. Show all design steps. Write verilog program of the same using structural modeling style. Also write verilog program of all components used in your design.	**14**
		OR	
Q.5		Design 4-bit full-adder with the help of 4 1-bit full-adders using structural model. Write verilog program for the same. Write module for 1-bit full adder also. Draw block diagram of your design.	**14**

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