Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME SEMESTER–IV • EXAMINATION – SUMMER 2015

Subject Code:740301 **Date: 05/12/2015**

Subject Name: Advanced VLSI Design

Time: 2:30 PM TO 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Appropriate comment lines are must in your program**

Q.1 An FIR filter operation is given by Y = Ax(n) + Bx(n-1) + Cx(n-2) +D x(n-3), where A, B, C, and D are filter coefficients and x(n) is input sample. Implement this operation using pipelined architecture having timing constraint of one 8bit x 8bit multiplier or one 8bit + 8bit adder only. Write verilog code and draw implementation diagram of your design. What is throughput and latency of your design ? **14**

Q.2(A) Draw implementation diagram of the following verilog statement. **07**

```
always @(posedge clk) begin
    Y<= A & B;
    Z<=  Y | C;
    Q<= Z & D;
end
```

How many clock cycles will be required to reflect any change in A to Q?

(B) Why asynchronous assert and synchronous deassert is used for reset circuit? With the help of verilog code and implementation diagram discuss it. **07**

OR

(B) With the help of verilog code and implementation diagram explain the use of multiple always blocks for flip-flop of different reset types. **07**

Q.3 Draw implementation diagram of the following verilog statements. Suggest improved implementation diagram to reduce area of the design using resource sharing concept for both statements. Consider statements are of different verilog programs. **09**

(i) assign Y= (S0==0)? A+B: (S1==1)? A+C: B+C; **05**

(ii) assign Y=S ? A+B : A+C;

OR

Q.3(A) With the help of verilog code and implementation diagram explain simple FSM and safe mode operated FSM. **07**

(B) What is the need of reordering of path? Explain it with necessary Verilog code and implementation diagram. **07**

Q.4(A) Implement the Boolean function Y=X7{X3(X1'+X2) + X6(X4'+X5)} using area as the constraint. Consider the synchronous set and reset (both active low) D-flipflops are available as FDS element in the FPGA. Write verilog code anddraw implementation diagram of the system. What are the throughput, latency and timing of your design? **07**

(B) Draw implementation diagram of the following verilog code **07**

```
wire A;
assign A=En0 ? !A:0;
assign Y=En1 ? A: 0;
```

OR

Q.4(A) Draw timing diagram of the simulation of x^3 implemented using pipelining. **07**

(B) Draw implementation diagram of the following verilog statement. **07**

```
always @(posedge clk) begin
    if (ctrl1) Y<=A;
    if(ctrl2)  Y<=B;
end
```

Q.5 Explain the use of FIFO structure to pass data between clock domains with the help of necessary state diagrams and block diagrams. **14**

OR

Q.5(A) Discuss different methods of optimal floor planning in detail. **07**

(B) Explain the impact of reset and set on area optimization in FPGA synthesis. **07**

****