GUJARAT TECHNOLOGICAL UNIVERSITY
PDDC - SEMESTER–III EXAMINATION – SUMMER 2016

Subject Code:X30901   **Date:26/05/2016**
Subject Name:Basic Electronics
Time:02:30 PM to 05:00 PM   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain V-I characteristics of P-N junction diode.	**7**
	(b)	Define the following terms: (i) Potential (ii) ev unit of energy (iii) Volt-equivalent temperature (iv) Thermal resistance (v) Intermodulation distortion (vi) Mean life time of a carrier (vii) Peak Inverse Voltage.	**7**

OR

Q.2	**(a)**	Define the rectification and describe the full wave bridge rectifier with the help of neat circuit diagram and waveforms.	**7**
	(b)	With circuit diagram and characteristics, explain input and output characteristics of transistor in common base mode.	**7**

OR

	(b)	Explain how D.C. load line is drawn on input characteristics of CE transistor configuration and state its importance.	**7**

Q.3	**(a)**	Define α and β in transistor and relation between α and β.	**7**
	(b)	Give a Comparison of CB, CC, CE transistor configuration.	**7**

OR

Q.3	**(a)**	Explain Voltage divider biasing method for transistor and prove the stability factor S=1 for voltage divider biasing method.	**7**
	(b)	Explain DC load line and Q-point for any transistor configuration. Also state the necessity of biasing and list biasing methods for transistor.	**7**

Q.4	**(a)**	Explain procedure to determine h-parameter hfe, hoe of transistor from static output characteristics.	**7**
	(b)	Define stabilization factors: S, S', and S". Derive expressions for S and S' for self-bias transistor circuit.	**7**

OR

Q.4	**(a)**	Draw a structure of p-channel MOSFET. Explain its working for enhancement type. Also draw and explain drain characteristics and transfer curve for the same device.	**7**
	(b)	Define thermal runaway. Derive necessary condition to avoid thermal runaway.	**7**

Q.5	**(a)**	Derive an expression for voltage gain (AV) for CS amplifier with an bypassed source resistance *RS*.	**7**
	(b)	Determine h-parameters for the two port network. Also draw the hybrid model for CE, CB and CC configurations.	**7**

OR

Q.5	**(a)**	List the basic configurations of a low frequency FET amplifier. Explain any one of them with the help of neat circuit diagram and small signal equivalent circuit.	**7**
	(b)	Draw class B push-pull system and show that the maximum conversion efficiency (η) is 78.5 % for this system.	**7**

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