Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–III EXAMINATION – SUMMER 2016

Subject Code:X31101 **Date:26/05/2016**

Subject Name:Advance Electronics

Time:02:30 PM to 05:30 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Write short note on Hybrid π model for a transistor in CE configuration and its circuit component.	**07**
	(b)	Classify the amplifiers based on position of quiescent point and also explain the distortion in amplifier.	**07**
Q.2	**(a)**	Derive the expression for the high 3-dB frequency f_H^* of n identical non-interacting stages in terms of f_H for one stage. Three identical cascaded stages have an overall upper 3-dB frequency of 20kHz and a lower 3-dB frequency of 20Hz. What are f_L and f_H of each stage? Assume noninteracting stages.	**07**
	(b)	List the steps required to carry out the analysis of feedback amplifier.	**07**
		OR	
	(b)	Draw and explain the two cascaded CE transistor stage. Derive necessary equation for it.	**07**
Q.3	**(a)**	For the voltage series feedback, obtain the expressions for input and output resistances R_{if} and R_{of}.	**07**
	(b)	Define slew rate of an op-amp and describe the technique to measure slew rate.	**07**
		OR	
Q.3	**(a)**	For FET source follower, with source resistance R, derive expressions for A_{vf}, R_{if}, R_{of}.	**07**
	(b)	Describe the operation of R-2R ladder DAC. How many bits are required to build R-2R DAC if reference voltage is 5V and DAC has resolution of 1 mV.	**07**
Q.4	**(a)**	State the conditions for an amplifier to work as an oscillator. How these conditions are fulfilled in a transistorized RC phase shift oscillator? Draw neat circuit diagram and derive the frequency of oscillation.	**07**
	(b)	Give the comparison between various logic families.	**07**
		OR	
Q.4	**(a)**	Draw the circuit diagram of Hartley oscillator and explain its working. Find the condition for oscillation.	**07**
	(b)	Draw two inputs TTL NAND gate with totem pole output. Explain its working and list advantages of it.	**07**
Q.5	**(a)**	Derive the expression for difference mode gain and common mode gain for a symmetrical emitter coupled differential amplifier.	**07**
	(b)	Draw and explain the working principle of Dual slope integrator ADC.	**07**
		OR	
Q.5	**(a)**	Define CMRR of differential amplifier. Show the circuit and explain how to measure CMRR of an op-amp.	**07**
	(b)	Describe the operation of counter type ADC with neat sketch.	**07**

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