Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI. EXAMINATION – SUMMER 2016

Subject Code:X61102 **Date:13/05/2016**

Subject Name:VLSI Technology and Design

Time:10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Define following operating regions for the MOS system with suitable energy band diagrams: **07**
(i) Accumulation (ii) Depletion (iii) Inversion

(b) Consider the following p-channel MOSFET process : **07**
Substrate doping $N_D = 10^{15}$ cm^{-3} , polysilicon gate doping density $N_D = 10^{20}$ cm^{-3} , gate oxide thickness $t_{ox} = 650$ A^o , and oxide interface charge density $N_{ox} = 2 \times 10^{10}$ cm^{-2} . Use $\varepsilon_{si} = 11.7\ \varepsilon_0$, $\varepsilon_{ox} = 3.97\ \varepsilon_0$ for the dielectric coefficients of silicon and silicon-dioxide , respectively.

(i) Calculate the threshold voltage V_{TO} , for V_{SB} = 0.

(ii) Determine the type and the amount of channel ion implantation which are necessary to achieve a threshold voltage of V_{TO} = - 2 V.

Q.2 **(a)** Discuss the effect of constant-voltage scaling on: **07**
(i) C_{ox} (ii) I_D (iii) P (iv) Power Density

(b) Explain MOS capacitance. **07**

OR

(b) Explain the following statements: **07**
(i) CMOS Inverter does not have substrate bias effects.
(ii) Voltage transfer characteristics of CMOS inverter can exhibit hysterisis when operated below certain supply voltage limit.

Q.3 **(a)** Define the following terms of an inverter with diagrams: **07**
(i) ζ_{PHL} (ii) ζ_{PLH} (iii) Rise time (iv) Fall time

(b) Draw CMOS implementation for following Boolean equation **07**

$$Z = \overline{(D + E + A)(B + C)}$$

Assume that $(W/L)_n = 10$ for all nMOS and $(W/L)_p = 15$ for all pMOS. Find $(W/L)_{equ}$ for nMOS and pMOS.

OR

Q.3 **(a)** Draw and explain working of CMOS inverter. Also Explain VTC of CMOS inverter. **07**

(b) Explain different Limitations imposed by Small-Device Geometries for NMOS. **07**

Q.4 **(a)** Write basic steps for NMOS fabrication steps. Explain LOCOS . **07**

	(b)	Draw and explain SR and JK latch using CMOS implementation.	**07**
		OR	
Q.4	**(a)**	Draw and explain NAND and NOR gate using CMOS implementation and depletion NMOS load implementation.	**07**
	(b)	Explain basic principal of pass transistor circuits. And also explain Voltage bootstrapping.	**07**
Q.5	**(a)**	Explain Latch-up in CMOS and also explain its prevention.	**07**
	(b)	Explain Ad hoc testable design techniques.	**07**
		OR	
Q.5	**(a)**	Explain PLD. Give difference between CPLD and FPGA.	**07**
	(b)	Explain controllability and observability. Also explain scan-based techniques.	**07**

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