Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VII EXAMINATION – SUMMER 2016

Subject Code:X71105 Date:05/05/2016

Subject Name: Embedded System (Departmental Elective-I)

Time:02:30 PM to 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Answer the following questions in short. (Two marks each)	**14**
	1	Give an example of hard real time system and soft real time system.	
	2	What is TDMI?	
	3	State criteria for selection of RTOS.	
	4	Which statement is true for RISC architecture among following? a. Instruction set is "orthogonal" b. Instructions are of variable length c. Load-and-Store Architecture d. All instructions execute in one clock cycle	
	5	Three tasks T1, T2, and T3 are having duration 25, 4, and 7 units respectively. If time slots are of 5 units then task T2 will be completed after which slot for given mechanism? a. Round robin scheduling b. First come first serve	
	6	Identify the addressing modes of the following instructions. a. LDR r0, [r1][r3] b. STMIA r1,{r2,r3,r4}	
	7	Explain context and context switching.	
Q.2	**(a)**	Describe the flow of cross development tools for ARM processor.	**07**
	(b)	Explain ARM programmer's model and CPSR format with diagram.	**07**
		OR	
	(b)	With the help of diagram, explain the organization of ARM with 3 stage pipeline.	**07**
Q.3	**(a)**	Explain following instructions. (i) LDMIA R2!,{R4-R8} (ii) ADD r3, r2, r1, LSL #3	**06**
	(b)	Discuss various data types supported by ARM processor.	**04**
	(c)	Explain multiply and accumulate operation with appropriate example.	**04**
		OR	
Q.3	**(a)**	Explain shift and rotate instructions of ARM processor.	**07**
	(b)	List various Exceptions and modes of ARM processor. How ARM handles exception?	**07**
Q.4	**(a)**	How do the following indicate the start and end of data frame? (a) UART, (b) HDLC, (c) CAN.	**07**
	(b)	Give detail characteristics of the Functions, ISR, and Task.	**07**
		OR	
Q.4	**(a)**	Write short note on ISA and PCI buses used for parallel communication between the networked I/O devices.	**07**
	(b)	Explain task and task states with appropriate example. Also discuss task control block.	**07**
Q.5	**(a)**	Discuss shared data problem with appropriate example. Discuss how semaphore can be used for share data problem?	**07**

	(b)	Compare process, task and thread. Explain multithreading mechanism in context of display process of mobile phone.	**07**

OR

Q.5	**(a)**	Explain Mutex. Also explain P and V semaphore with appropriate example.	**07**
	(b)	Describe process management and memory management service of RTOS.	**07**

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