Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–II EXAMINATION – WINTER 2015

Subject Code: X21102 **Date:28/12/2015**

Subject Name: Digital Logic Design

Time: 02:30pm to 05:00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Design a combinational circuit that converts 4 bit Binary code to 4 bit Gray code using EX-OR gates.	**07**
	b)	1. Perform the subtraction using 10's Complement method: 3570 - 2100	**03**
		2. Simplify the Boolean function to minimum number of literals: $XY + \overline{X}Z + YZ$	**02**
		3. Find the Complement of functions: $F_1 = \overline{X}Y\overline{Z} + \overline{X}\,\overline{Y}Z$ $F_2 = X(\overline{Y}\,\overline{Z} + YZ)$	**02**
Q.2	**(a)**	Do as directed: (a) $(1010.011)_2 = (\quad)_{10}$ (b) $(2AC5.D)_{16} = (\quad)_2$ (c) $(623.77)_8 = (\quad)_{16}$ (d) Find the 2's Complement number of 1010101. (e) $(225.225)_{10} = (\quad)_2$ (f) State the duality principle. (g) $(11010)_2 - (1101)_2 = (\quad)_2$	**07**
	(b)	Prove with figure that NAND and NOR are Universal Gates.	**07**
		OR	
	(b)	Implement and explain 4 * 16 Decoder using five 2 * 4 Decoder circuit.	**07**
Q.3	**(a)**	Simplify the following Boolean function in (a) sum of products (b) Product of sums and implement it by using Universal Gates. F (A, B, C, D) = ∑ (0, 1, 2, 5, 8, 9, 10)	**07**
	(b)	Implement the Boolean function by using 8 * 1 multiplexer as well as NOT gate F(W, X, Y, Z) = ∑(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)	**07**
		OR	
Q.3	**(a)**	Determine the prime implicants of the function using tabulation method F(W, X, Y, Z) = ∑(1, 4, 6, 7, 8, 9, 10, 11, 15)	**07**
	(b)	Explain Random access memory in detail.	**07**
Q.4	**(a)**	Construct and explain mod-6 synchronous counter using JK flip flop.	**07**
	(b)	List types of shift register and explain in brief.	**07**
		OR	
Q.4	**(a)**	Design BCD ripple counter using Toggle flip flop.	**07**
	(b)	Convert D flip flop to JK flip flop as well as JK flip flop to D flip flop and explain it in brief.	**07**
Q.5	**(a)**	Define: Integrated circuit and briefly explain SSI, MSI, LSI and VLSI	**07**
	(b)	Give classification of Logic families and compare CMOS and TTL families.	
		OR	

Q.5	**(a)**	What is race around condition? Explain the Master slave JK Flip flop.	**07**
	(b)	Explain in brief: Arithmetic logic unit	**07**