Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**PDDC - SEMESTER–III EXAMINATION – WINTER 2015**

**Subject Code:X30902** **Date:21/12/2015**

**Subject Name:Analog & Digital Electronics**

**Time: 10:30pm to 01:00pm** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | Write down about any seven characteristics of an ideal & a practical Op Amp. | **07** |
| | **(b)** | Draw the block diagram representation of a typical operational amplifier and justify the significance of each block. Also plot the transfer characteristics of an Op Amp. | **07** |
| **Q.2** | **(a)** | Design an Op Amp circuit for obtaining $V_O=V_1-2V_2$. | **07** |
| | **(b)** | Derive the equation of time period for IC 555 in astable mode of operation. | **07** |
| | | **OR** | |
| | **(b)** | Derive the equation of time period for IC 555 in monostable mode of operation. | **07** |
| **Q.3** | **(a)** | Define minterms, maxterms, Product of Sums and Sum of Products. Simplify (B + BC).(B + B´C). | **07** |
| | **(b)** | What are binary numbers? How are they different from BCD numbers? List all 4 digit binary and BCD numbers. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | (1) A (B + C) = _____<br>(2) A + A.B = _____<br>(3) A.0 = _____<br>(4) A + A' = _____<br>(5) (A + B)' = _____<br>(6) A + 1 = _____<br>(7) 1.1 = _____ | **07** |
| | **(b)** | Draw the equivalent circuit of an AND gate using NOR gate & an OR gate using NAND gates only. | **07** |
| **Q.4** | **(a)** | Do as directed:<br>(1) Convert $4B00_{16}=(\ )_8=(\ )_4=(\ )_2=(\ )_{10}$<br>(2) Given $(16)_{10}=(10000)_b$, find the value of b. | **07** |
| | **(b)** | (1) A+BC = _____<br>(2) A.(A+B) = _____<br>(3) A.0= _____<br>(4) A .A' = _____<br>(5) (A. B)' = _____<br>(6) A .1 = _____<br>(7) 1+1 = _____ | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Using K map technique, minimize<br>(1) $G(A,B,C)= \sum m(0,1,2) + d(3,5)$<br>(2) $G(A,B,C)= \sum m(4) + d(6,7)$ | **07** |
| | **(b)** | Implement a half Adder/ half Subtractor circuit with its truth table and circuit. | **07** |

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|---|---|---|---|
| **Q.5** | **(a)** | Define Flip flop. Classify Flip flop circuits. Explain in details about any one of them. | **07** |
| | **(b)** | Define Counter. Classify Counters. Explain any one of them in details. | **07** |

**OR**

| | | | |
|---|---|---|---|
| **Q.5** | **(a)** | Draw the block diagrams of encoders, decoders, multiplexers and de multiplexers with their truth tables. | **07** |
| | **(b)** | Define Shift Registers. Classify all the types of shift registers. Explain any one of them. | **07** |

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