Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI EXAMINATION – WINTER 2015

Subject Code:X61102 **Date:12/12/2015**

Subject Name: VLSI Technology and Design

Time: 02:30pm to 05:00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	1) Give difference between semicustom and full custom design. 2) Give difference between FPGA and Gate array design.	**07**
	(b)	Explain important of CAD tolls for different abstraction level of design.	**07**
Q.2	**(a)**	Explain fabrication steps for n-well CMOS process with necessary sketches.	**07**
	(b)	Explain concept of threshold voltage of nMOS. Also explain effect of substrate bias effect of threshold voltage.	**07**
		OR	
	(b)	Explain MOS Capacitance.	**07**
Q.3	**(a)**	A CMOS inverter has $V_{TO,n}$ = 0.8 V, $V_{TO,p}$ = - 0.8 V , and k_n=k_p. Obtain NM_H and NM_L for V_{DD} = 10v .	**07**
	(b)	An NMOS transistor has μ_n = 70 cm^2/ VS, C_{ox} = 8. 10^{-8} F/ cm^2, $V_{TO,n}$ = 0.78 V, W_n = 20um, L_n= 2um to calculate drain current for V_{GS} = 2V and V_{DS}= 1V.	**07**
		OR	
Q.3	**(a)**	Define T_{PLH} and T_{PHL}. Derive equation of T_{PHL} for CMOS inverter.	**07**
	(b)	Derive equation for dynamic power consumption for CMOS inverter.	**07**
Q.4	**(a)**	Draw CMOS and depletion NMOS load implementation for following Boolean equation 1) $Z = \overline{ABE + DC}$ 2) $Z = \overline{A + BE + DC}$	**07**
	(b)	Draw CMOS implementation for $Z = \overline{A(D + E) + BC}$. Find Euler path and draw stick diagram for this CMOS implementation.	**07**
		OR	
Q.4	**(a)**	Explain CMOS Latch up problems. List prevention for it.	**07**
Q.4	**(b)**	Explain on chip clock generation and distribution	**07**
Q.5	**(a)**	Explain Ad hoc testable design techniques.	**07**
	(b)	Explain different fault types and models.	**07**
Q.5	**(a)**	Draw and explain CMOS implementation of D flips flop.	**07**
	(b)	Explain NORA CMOS logic.	**07**

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