
By Dr. Vijaykrishnan Narayanan
Department of Computer Science & Engineering, Penn State, USA

Date: 31 July – 2 August, 2015

Venue: Gujarat Technological University
Nr. Vishwakarma Government Engineering College
Nr. Visat Three Roads, Visat - Gandhinagar Highway
Chandkheda, Ahmedabad – 382424 – Gujarat
Under the visionary leadership of Honorable Vice Chancellor, Dr. Akshai Aggarwal, Gujarat Technological University successfully organized Three Day Workshop on “Power Aware Computing, Intelligent Camera Systems & Trends in Computer Architecture” from 31st July to 2nd August, 2015 at its Chandkheda Campus, Ahmedabad. The workshop was conducted by Dr. Vijaykrishnan Narayanan from The Pennsylvania State University, USA. The core objective of the workshop was to give insight about the current trends in computer architecture in order to upgrade the knowledge by demonstrating practical applications to the faculty and students of engineering discipline.

About Resource Person:
Dr. Vijaykrishnan Narayanan is currently at the Computer Science and Engineering and Electrical Engineering Departments at Penn State. He is a member of the Embedded and Mobile Computing Design Center and his research/teaching interests are in the areas of energy-aware reliable systems, embedded systems, on-chip networks, system design using emerging technologies (3D and Nano) and computer architecture. His research is supported by grants from National Science Foundation, The Technology Collaborative, and DARPA. Dr. Narayanan has received several awards including the Penn State Engineering Society Outstanding Research Award in 2006, IEEE CAS VLSI Transactions Best Paper Award in 2002, the Penn State CSE Faculty Teaching Award in 2002, and many more. His research interests are Energy-Aware and Reliable Systems, Embedded Java, Nano/VLSI Systems, Computer Architecture.

**DAY – 1 (31TH JULY, 2015)**

The workshop commenced with welcome speech by Ms. Nidhi Thakore - Program Coordinator. Inaugural session was graced by Mr. Naresh Jadeja - Deputy Director GTU and he shared the vision of Honourable Vice Chancellor and delivered encouraging words to the participants by motivating them to attend such engineering workshops to be in pace with the changing trends. He also explained the objectives, importance of organizing such computer oriented workshop and suggested students can explore in this area and can work upon it for their final year project. Mr. Jadeja warmly welcomed Dr. Narayanan with a flower bouquet.

Technical session was delivered by Dr. Narayanan. Following topics were discussed in brief on the first day:

- Cloud and Data Center
- Ultra Low Power and Reliable Systems
- Multicore Systems, Network on Chip, Parallel Software
Embedded Systems
Emerging Technologies Nanoarchitectures and Stacked 3D design
Low power Devices
Soft errors and Neutron Detectors
Cores to Embedded Systems
Vision Processing Framework
Computer Architecture and its applications in Cell Phones, Game Consoles (Xbox, Wii, Playstation), Television Sets, Tablets (iPad, Galaxy, Kindle), Laptops, Desktops, Printers/Cameras/Microwaves/Cars
Processor Terminology like CPUs (Intel Core 2), GPUs (Nvidia GeForce GTX 590), System-on-Chip (SoC) (Apple A5), ASICs (special purpose chips), FPGAs (Xilinx Virtex 7), DSPs (TI C6000 series), Microcontrollers (Freescale S12), ASIP (Tensilica Xtensa 9)
Classes of computer like Desktop computers (incl. laptop, netbooks, ultrabooks), Servers, Supercomputers, Embedded computers, Embedded processors
Characteristics of Embedded Processors
Cloud Computing/Warehouse Computing
Moore’s Law
Multicores
Hardware Security
New Interconnect Technologies
Chip level 3D Integration
Various challenges in computer architecture like Power Consumption, Parameter Variations, Economics, Wires, I/O Bandwidth, Aging Effects and Early Wearout, Design Costs, Transient Errors and Programming Parallel Architectures

DAY – 2 (1ST AUGUST, 2015)

Session of Intelligent Camera Systems

Dr. Narayanan focused on the following:

- Smart Glasses: Visual Cortex on Silicon
- ThirdEye for Visually Impaired
- Building Computational Models of Brain
- ThirdEye Prototypes
- ThirdEye with Augmented Reality
- Embedded Vision Design Platform
- Sensor Fusion
On the last day of the workshop, Dr. Narayanan focused on Digital Design using FPGAs and discussed the following in brief:

- Introducing Verilog which is based on C, originally Cadence proprietary, now an IEEE Standard. It is easier to learn, read, and design compared to VHDL
- Hardware Description Languages which allows design specification at the Register Transfer Level (RTL)
- RTL that describes the dataflow from Registers, to Combinatorial Logic, to Registers
- VHSIC (Very High Speed Integrated Circuit) Hardware Description Language developed by the US Department of Defense and which is more formal than Verilog and has more features than Verilog.
- Various kinds of flip-flops along with their properties.

The workshop ended with vote of thanks by Ms. Nidhi Thakore. Overall it was very interactive with the discussion of the expert with the participants and the feedback from the workshop was extremely positive.
FEEDBACK

“The workshop organized was one of a kind with the resource person having a plethora of knowledge. Looking forward to more such opportunities.”

--Manoranjan Padhy, Parul Institute of Engineering and Management

“First of all thank you for a wonderful workshop We got to learn many new things of which we were least aware and scope in our field We all are further looking for the workshops like this in which experts can tell us about the real application of our subjects.”

--Sushmitha Mudaliar, GEC Gandhinagar

“The workshop was very nice and helpful to understand how the processors work and how to select the processor for the different use after this workshop. Also we also feel very proud to learn from such as good speaker/professor.”

--Meet, Vadodara Institute of Engineering

“The workshop really proved to be very useful for enlightening our knowledge in the field of computer architecture, intelligent camera and power computing. It was a great time learning such important and modern research concepts from Prof. Vijaykrishnan, I hope that such type of workshop should be continued in the future to continue the spirit of learning.”

--Suraj Pandey, GEC Gandhinagar

“This may be first seminar of GTU in which faculty gave us homework to go deep in the subject and faculty also tried his best to give use knowledge of subject from basic to high level. I would like to attend this kind of workshop ever and ever.”

--Indresh Agrawal, UCET

“Excellent workshop. Got new trends in digital logic design. Excellent speaker and actively participated students. I heartily thank Dr. Narayanan Sir and the whole GTU team who arranged it so well for participants. Thank you!”

--Vrajesh D. Patel, Asst. Professor, I.I.E.T- DHRAMAJ